Amendments to the Abstract:

Applicants amend the Abstract as follows:

A method for processing registers in an out-of-order processor. The technique substantially simultaneously reads values from a plurality of registers. A particular instruction is parsed. A select number of registers to be modified is determined by the instruction. The selected number of registers is modified. The values are substantially simultaneously written to the plurality of registers. ~~A predicate in an instruction is predicted. An architecturally correct value is then computed using a read-modify-write operation. The predicted value is compared to the architecturally correct value. The instruction with an incorrectly predicted predicate is flushed from the pipeline if the predicted value and the architecturally correct value are different.~~